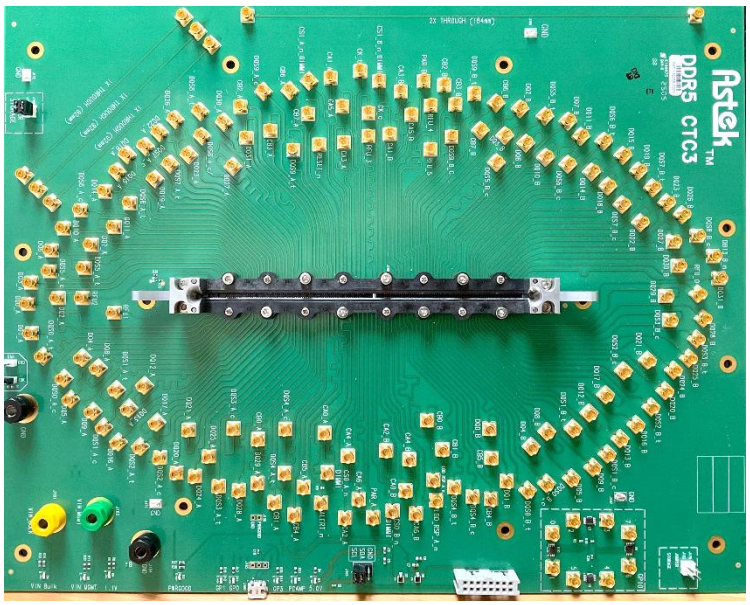
A9-CTC3

User Manual

Version: **December 1, 2025**



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1 Contents

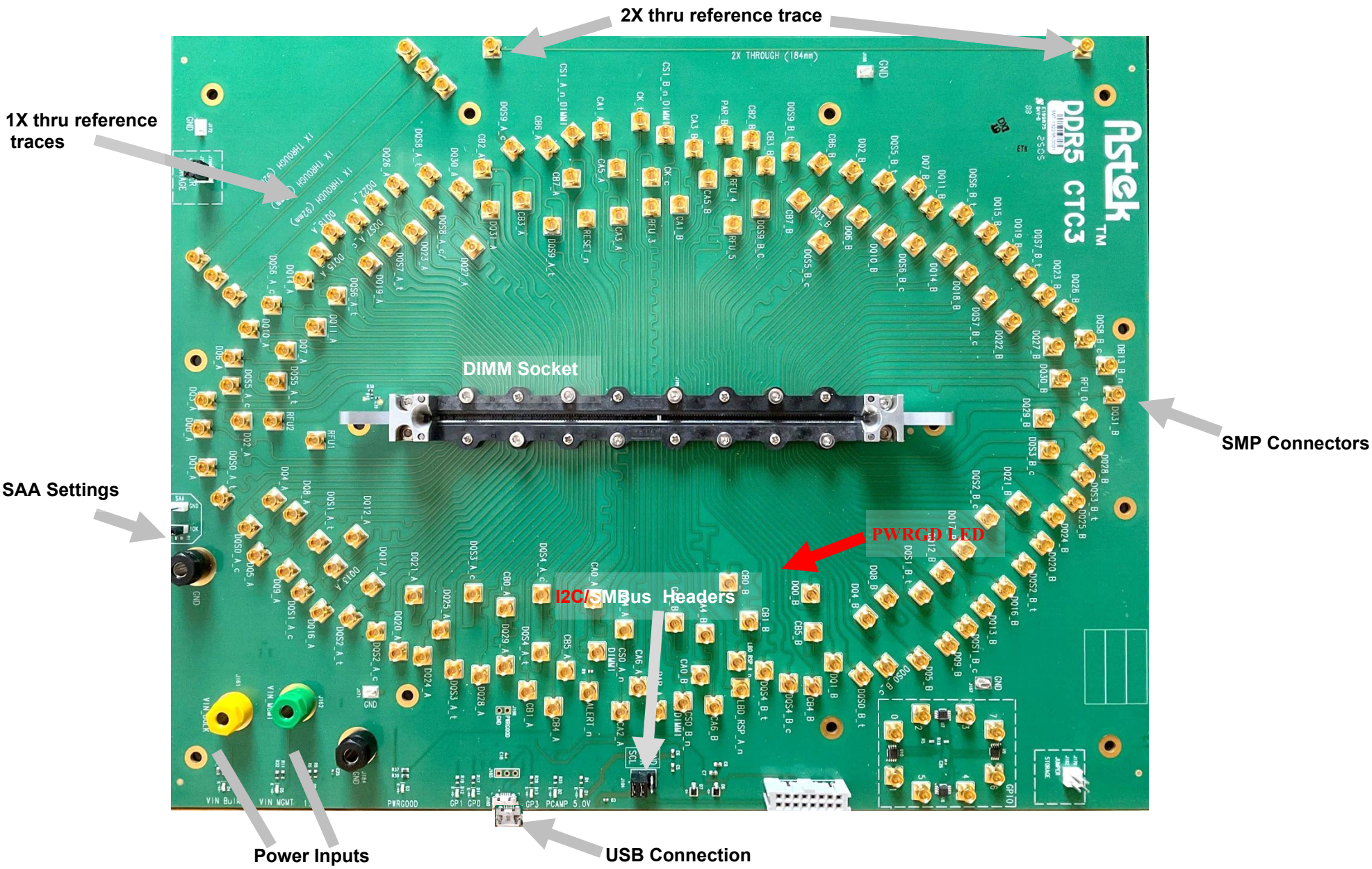
2 Introduction / Overview

This document outlines the features and use of Astek's Channel Test Card 3 (CTC3). The CTC3 provides signal access for testing DDR5 DIMMs, MRDIMMs and component test cards using oscilloscopes, BERTs, and signal generating test equipment. The CTC3 provides access via SMP connectors to all signals on a 287 pin DIMM connector. The CTC3 is available in three configurations high-performance socket, standard socket and no DIMM socket.

Each high-speed signal path is 50-Ohms and matched to within +/- 1mil in length. See table on page 4 for a complete listing of signal routed to SMP connectors.

Features

- All high-speed signals brought out to high-performance SMP connectors.
- All signals are matched to within 1 ps.
- MRDIMM gold finger # 220 not connected.
- High performance/high reliability MRDIMM Test connectors (>1000s of insertions)
- Supports MRDIMM testing AND test card testing (RVC2 test card, etc.)
- I2C control via USB
- VIN_BULK and VIN_MGMT external Power Supply inputs
- 1x and 2x reference traces for BERT and scope calibration
- Sixteen (16) General Purpose I/Os (aka RESET, CS[1:0],.,.,)


2X thru reference trace
1X thru reference traces
DIMM Socket
SMP Connectors
SAA Settings
PWRGD LED
I2C/SMBus Headers
Power Inputs
USB Connection

3 Optional Equipment

Astek RDIMM Parametric Card

The RDIMM Parametric Card can be used for advanced characterization of the CTC3 board and is useful for changing the reference plane to other locations in the test system.

Astek DDR5 RDIMM RCD Test Card

A versatile RDIMM test card focused on Gen5 Registering Clock Driver (RCD05) test, providing. access to all I/O's DCA_A/B, Q(A/B)CA_A and Q(A/B)CA_B inputs and outputs of the RCD05.

Astek DDR5 RDIMM Replica Channel Test Card

DDR5 Replica Channel Card (RPLC) is a RDIMM receiver test calibration tool. Several "Trace Sets" consisting of a differential clock (CK or DQS) and associated single ended signal (CA/CS or DQ) are included on the RPLC, to emulate the signal paths on DDR5 Raw Card (JEDEC) DIMMs

Micro USB cable

A micro USB cable can be used to connect the CTC3 to a host PC. The USB interface provides a method of configuring a DIMM or test card during characterization testing.

SMP cabling

SMP cables are needed to connect the CTC3 to test equipment or other test hardware. Depending on the equipment and connectivity needs, either SMP to SMP cables or SMP to SMA cables are needed.

Power Supply

A dual-port power supply is required to power the device under test. For RDIMM cards, V Management 3.3V and V Bulk 12V are required.

Test equipment

Depending on the characterization needs, various test equipment such as oscilloscopes, bit-error rate testers (BERTs), and arbitrary waveform generators are used to drive stimulus and monitor outputs of devices under test.

I2C Host

CTC3 Controller Software provides a register interface and scripting language useful for initializing and controlling device under test (see CTC3 Controller Software User Guide).

Contact your Astek representative for information and quotations for the optional equipment listed

4 Powering the CTC3

The CTC3 is designed to support testing of RDIMMs requiring 3.3V and 12V, component test cards. Power for the device under test is applied to appropriate banana jacks located at lower left corner of CTC3 Test Fixture.

Voltage Pin	Voltage Level	Banana Jack	Color
VIN BULK	12V	12V	Yellow
VIN MGMT	3.3V	3.3V	Green
GND	0V	0V	Black

Presence of VIN_MGMT and VIN_BULK are enunciated respective LEDs. When a CTC3 is connected to a PC via USB cable, 1.1V and 5.0V LEDs will be lit. USB traffic is enunciated by GP3 LED near USB cable connector. GP3 LED blinks when PC to CTC3 traffic is detected.

5 Signals Probed

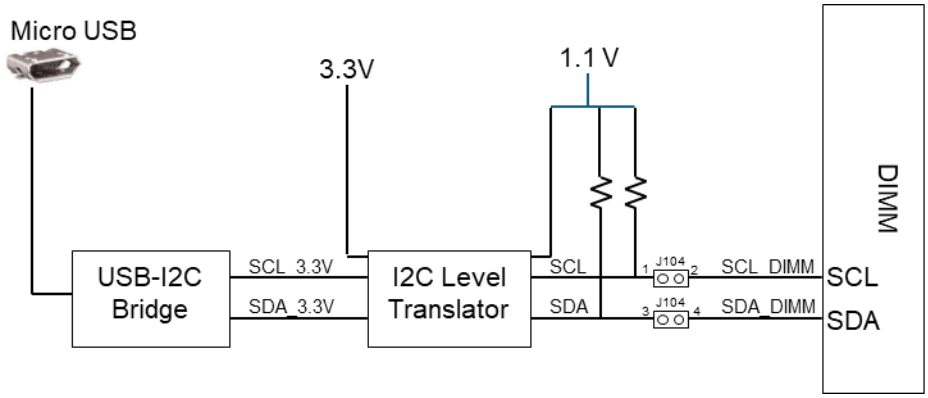
The following signals are brought out to SMP Connectors on the CTC3

Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin
ALERT_n	62	CB0_A	51	CK_c	218	DQ0_A	7	DQ10_A	163	DQ21_A	38	DQS0_A_c	12	DQS5_A_c	156
CA0_A	66	CB0_B	96	CK_t	217	DQ0_B	100	DQ10_B	256	DQ21_B	131	DQS0_A_t	11	DQS5_A_t	157
CA0_B	76	CB1_A	53	CS0_A_n	64	DQ1_A	9	DQ11_A	165	DQ22_A	181	DQS0_B_c	105	DQS5_B_c	249
CA1_A	211	CB1_B	98	CS0_B_n	84	DQ1_B	102	DQ11_B	258	DQ22_B	274	DQS0_B_t	104	DQS5_B_t	250
CA1_B	221	CB2_A	196	CS1_A_n	209	DQ2_A	152	DQ12_A	25	DQ23_A	183	DQS1_A_c	23	DQS6_A_c	167
CA2_A	68	CB2_B	241	CS1_B_n	229	DQ2_B	245	DQ12_B	118	DQ23_B	276	DQS1_A_t	22	DQS6_A_t	168
CA2_B	78	CB3_A	198	PAR_A	74	DQ3_A	154	DQ13_A	27	DQ24_A	40	DQS1_B_c	116	DQS6_B_c	260
CA3_A	213	CB3_B	243	PAR_B	227	DQ3_B	247	DQ13_B	120	DQ24_B	133	DQS1_B_t	115	DQS6_B_t	261
CA3_B	223	CB4_A	58	RESET_n	207	DQ4_A	14	DQ14_A	170	DQ25_A	42	DQS2_A_c	34	DQS7_A_c	178
CA4_A	70	CB4_B	89	LBD	86	DQ4_B	107	DQ14_B	263	DQ25_B	135	DQS2_A_t	33	DQS7_A_t	179
CA4_B	80	CB5_A	60	LBS	87	DQ5_A	16	DQ15_A	172	DQ26_A	185	DQS2_B_c	127	DQS7_B_c	271
CA5_A	215	CB5_B	91	RFU_0	144	DQ5_B	109	DQ15_B	265	DQ26_B	278	DQS2_B_t	126	DQS7_B_t	272
CA5_B	225	CB6_A	203	RFU_1	149	DQ6_A	159	DQ16_A	29	DQ27_A	187	DQS3_A_c	45	DQS8_A_c	189
CA6_A	72	CB6_B	234	RFU_2	150	DQ6_B	252	DQ16_B	122	DQ27_B	280	DQS3_A_t	44	DQS8_A_t	190
CA6_B	82	CB7_A	205	RFU_3		DQ7_A	161	DQ17_A	31	DQ28_A	47	DQS3_B_c	138	DQS8_B_c	282
		CB7_B	236	RFU_4	231	DQ7_B	254	DQ17_B	124	DQ28_B	140	DQS3_B_t	137	DQS8_B_t	283
				RFU_5	232	DQ8_A	18	DQ18_A	174	DQ29_A	49	DQS4_A_c	56	DQS9_A_c	200
				FAIL_n	147	DQ8_B	111	DQ18_B	267	DQ29_B	142	DQS4_A_t	55	DQS9_A_t	201
						DQ9_A	20	DQ19_A	176	DQ30_A	192	DQS4_B_c	238	DQS9_B_c	94
						DQ9_B	113	DQ19_B	269	DQ30_B	285	DQS4_B_t	239	DQS9_B_t	93
								DQ20_A	36	DQ31_A	194				
								DQ20_B	129	DQ31_B	287				

6 I2C

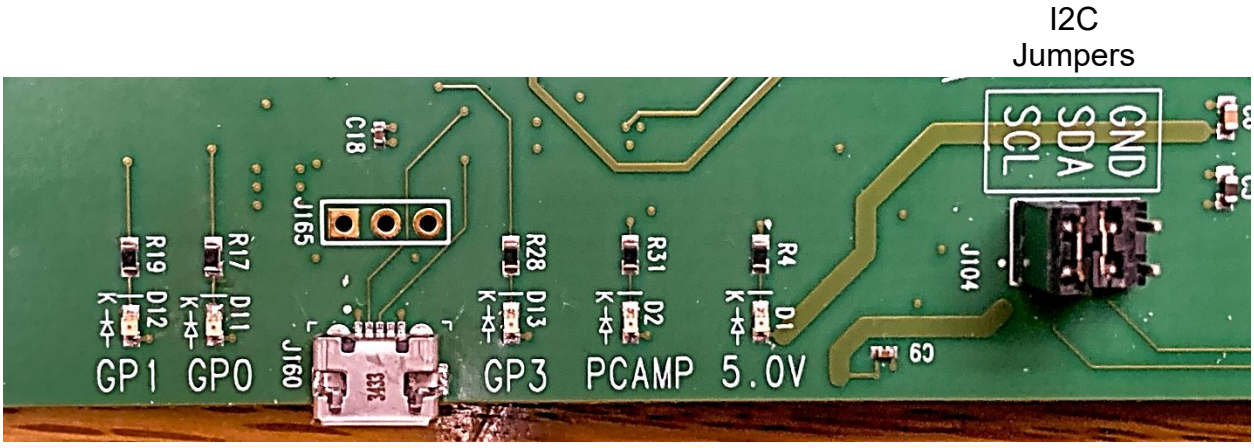
I2C Circuitry

Block Diagram of the I2C circuitry on the CTC3 is shown below.



Micro B USB connector provides access to CTC3's SM Bus. (DIMM socket: SDA – Pin 5, SCL – Pin 4)

The location of the USB Micro B connector and I2C support circuitry is shown below.

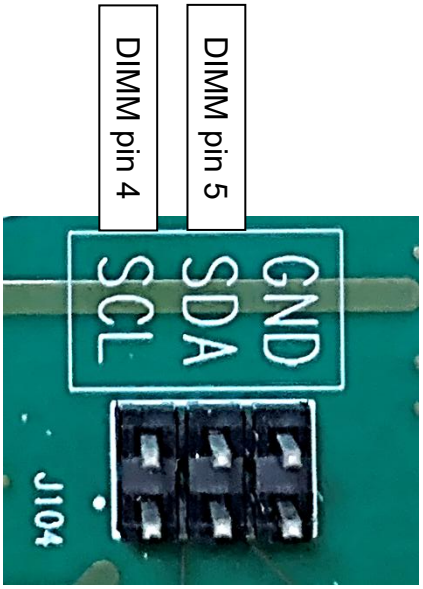


USB Connector

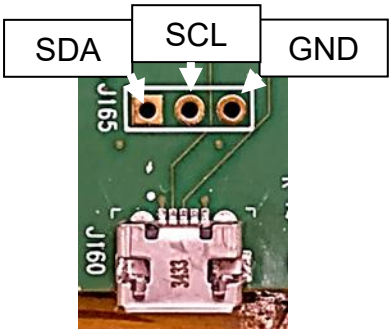
The I2C_VCC pull-up voltage is set at 1.1V.

By default, jumper J104 installed. When J104 is installed, the I2C bus is driven via the USB-to-I2C bridge.

To access DDR5 DIMM I2C pins directly, remove J104 to attach directly to I2C pins as shown below. When the jumpers are removed, on-board pullups are also disconnected from the circuit (see the block diagram above).



The 3.3V side of the I2C/SM Bus may be probed directly with an oscilloscope or protocol analyzer at location J165



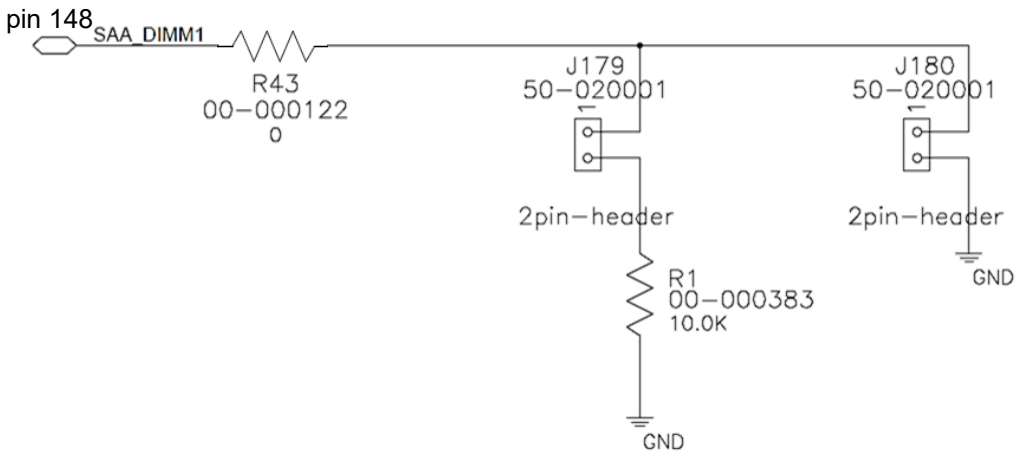
The pinout of J165 is:

Pin	Signal
1	SDA
2	SCL
3	GND

SAA Circuitry

The SAA pin circuitry on the CTC3 provides the option to change the address of the DIMM socket. Jumpers J179 or J180 determine the DIMMs HOSTID.

The SAA circuitry is shown below.



The following table shows the relationship between resistor value R1and HOSTID.

Resistor Value		**Meaning**
10,000 Ω	(R1)	HOST ID = 000 (default)
15,400 Ω	(R1)	HOST ID = 001
23,200 Ω	(R1)	HOST ID = 010
35,700 Ω	(R1)	HOST ID = 011
54,900 Ω	(R1)	HOST ID = 100
84,500 Ω	(R1)	HOST ID = 101
127,000 Ω	(R1)	HOST ID = 110
196,000 Ω	(R1)	HOST ID = 111
VSS	(J180)	HOST ID = 000

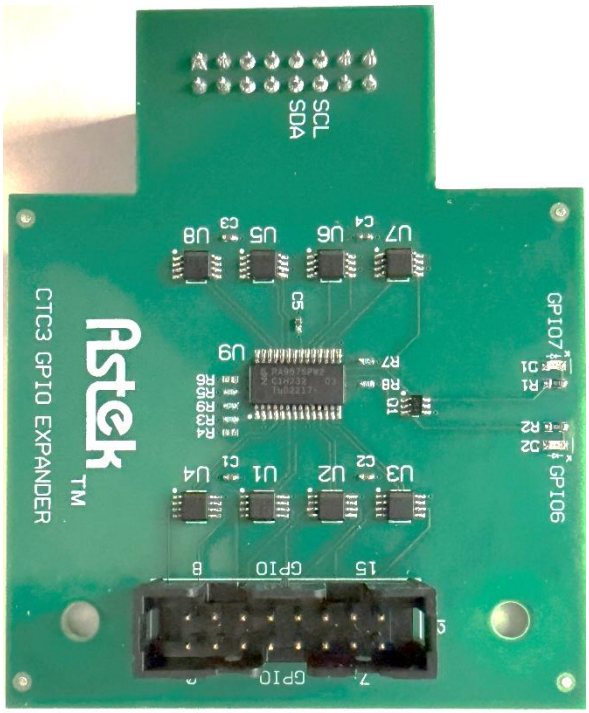
To use a R1 to select the HOSTID, install J179 (default location) and change R1 to the desired value. R1 is located near J179.

To set the HOST ID = 0, install J180.

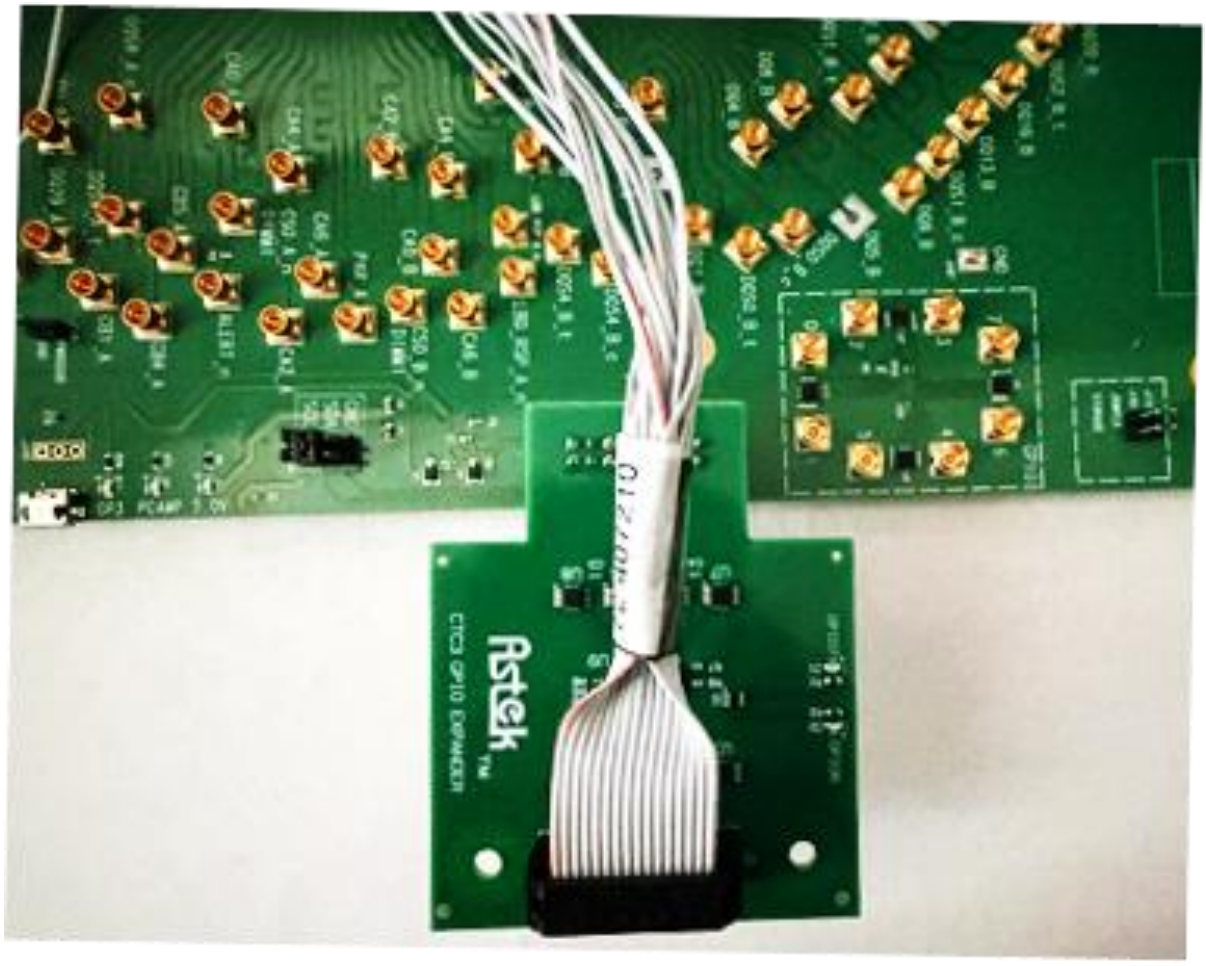
SAA R43 is located on CTC3's bottom side near 287 pin DIMM socket.

7 GPIO

The GPIO Expander Interface provides control of sixteen (16) I/O lines used to establish initial conditions of the device undertest.



GPIO Expander card plugs into connector J177 (2X8 socket) on the front edge of the CTC3 board.



Expander card interfaces with SMP signal connectors on the CTC3 via the 2X8 to SMP interface cable included with the CTC3 and GPIO expander card.

User control of GPIO output Ports is programmed over CTC3's I2C SM Bus. PC based CTC3 Controller Software controls CTC3's I2C SM Bus over CTC3's USB interface. Each GPIO port can be independently programed to logic Low, or High on a Port-by-Port basis. Port output levels are 0V Low to 1.1V High.

Port programming example:

Set Port 0 to logic level High.

DDR5CNTRL Setgpio 0 On

Setting GPIO 0 off, switches GPIO 0 to logic level Low.

8 Calibration Traces

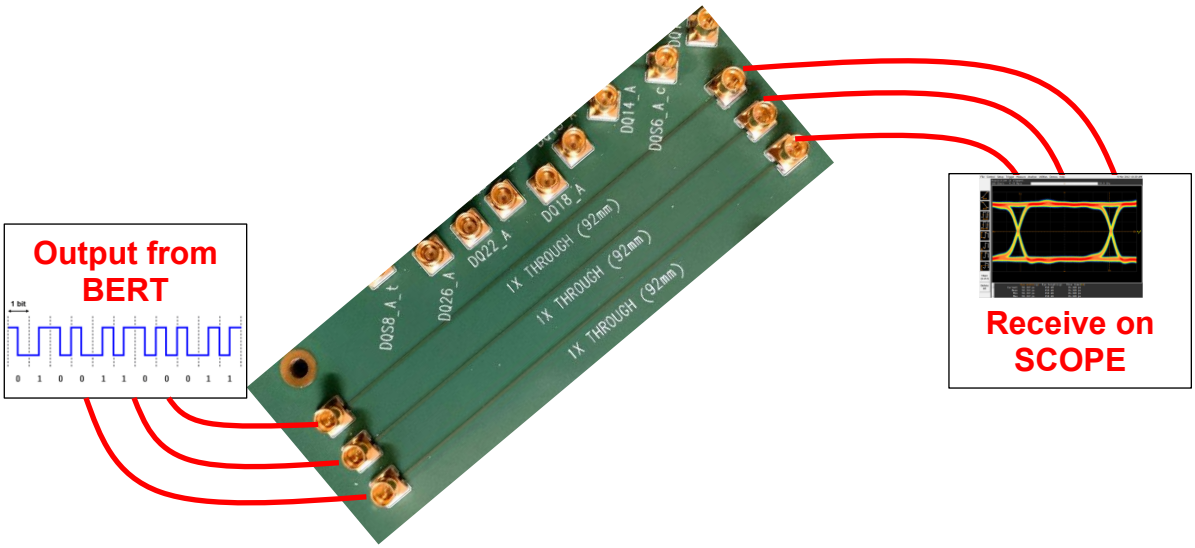
There are two calibration structures on the CTC3.

- 1X THRU three 50 Ohm paths
- 2X THRU One 50 Ohm path

1X THRU

The 1X THRU calibration structures are used when calibrating and configuring a BERT. The three paths allow calibration of one DQ and one DQS pair at the same time.

A typical calibration setup is shown below.



The 1X THRU trace is the same length as CTC3 traces from a SMP to DIMM socket Therefore, this calibration structure allows the user to “view” the signal as observed at the DIMM socket pin, for example path DQ0_A SMP to DIMM socket pin 7. This provides an improved calibration of the signal from the BERT to a DIMM since it take into account losses across CTC3’s PCB traces.

Additional techniques such as de-embedded CTC3 trace loss effects can be used to move the reference point closer to a BGA ball of a DRAM.

2X THRU

The 2X THRU calibration structure is used to generate s-parameters of traces on the CTC3. The 2X THRU structure is measured and then divided in half. This results in an s-parameter with one SMP and one length of signal trace. The s-parameter can be used for de-embedding of a scope or similar equipment.

9 Ordering Information

The following part numbers are helpful when ordering from Astek. Contact Astek representative for quoting and availability.

Part Number	Description
A9-CTC3-01	DDR5 CTC3 with high-reliability socket installed
A9-CTC3-02	DDR5 CTC3 with standard socket installed
A9-CTC3-03	DDR5 CTC3 with NO socket installed

Additional products related to the CTC3 are available from Astek.

Part Number	Description
A9-DIMM5-01	DDR5 RDIMM Parametric Test Card
A9-UDIMM5-01	DDR5 UDIMM Parametric Card
A9-UDIMM-01	UDIMM Riser Card
A9-CNTL-01	DDR5 Controller Board w/ RCD and Reset Automation
A9-RCD-01	DDR5 Registering Clock Driver (RCD) Test Card
A9-WCNTL-01	DDR5 Controller dual - Channel
A9-CMBO-01	DDR5 X8 Combination Test Card (8 bit memory)
A9-X16 Combo-01	DDR5 X16 Combo Card (16 bit memory)
A9-RPLC-01	DDR5 Replica Channel Card
A9-SIT-01	DDR5 RCD Signal Integrity Card
A9-CKD-01	DDR5 Clock Driver Test Card
A9-RVC2-01	DDR5 RDIMM RCD Test Card
A9-A2PCBL-1000	SMA to SMP cable, 1.0m
A9-A2PCBL-1000P	SMA to SMP cable, 1.0m, matched pair
A9-A2PCBL-0500	SMP to SMP cable, 0.5m
A9-A2PCBL-0500P	SMP to SMP cable, 0.5m, matched pair

Part Number	Description
A9-CTC3-SW-01	CTC3 Controller Software-

10 How to Contact Astek Corporation

Astek Corporation may be contacted by the following methods:

PHONE: (719) 260-1625 (USA)

FAX: (719) 260-1668 (USA)

EMAIL: support@astekcorp.com

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