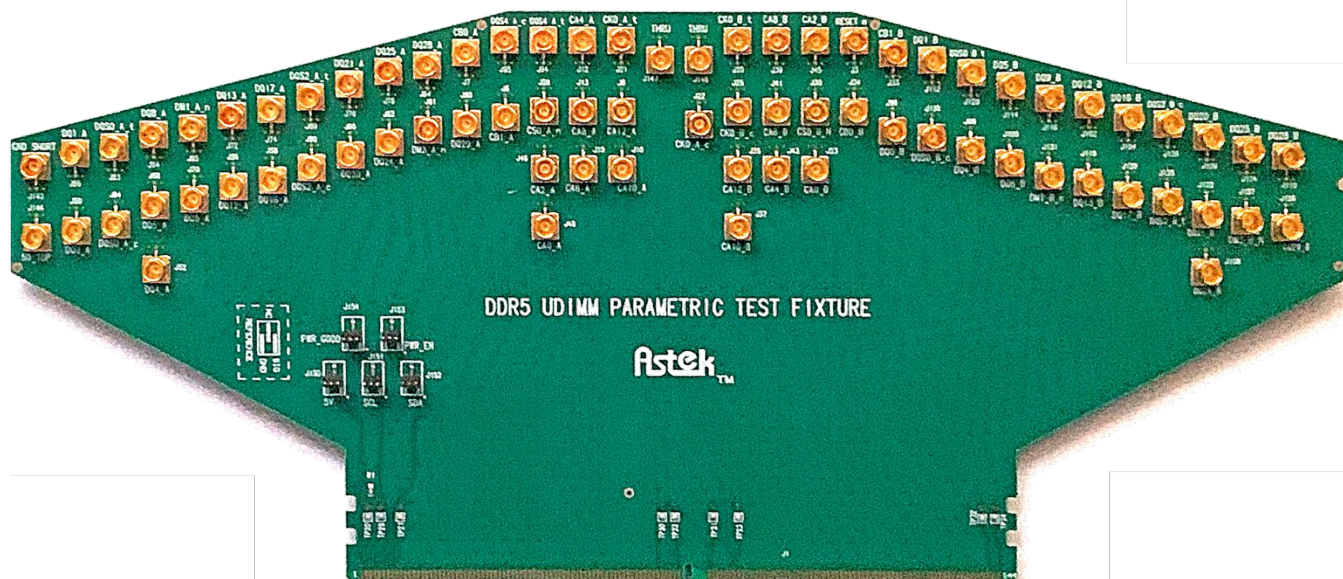


DDR5 UDIMM Parametric Card

A9-UDIMM5-01 Product Brief



UDIMM Parametric C

DDR5 UDIMM Parametric Test Fixture

The DDR5 UDIMM Parametric Card enables designers to access all signals from a DDR5 UDIMM slot by plugging the DDR5 UDIMM Parametric Card directly into the UDIMM slot on a host. The test fixture is constructed from high speed, low loss MEGTRON 6 board material.

Technical Specification

UDIMM Signal Count: 145

- All high-speed signals are brought out to SMP connectors
 - Traces are length matched to within 1 mil.
- Low speed signals are brought out to 50 mil headers
- VIN Bulk and VIN Management are brought out to 50 mil headers

Calibration Structures:

- 2X THRU
- 1X SHORT
- 1X OPEN
- 1X 50Ω LOAD

Approximate Size: 262.9mm x 114.3mm

Connectors: SMP (high-speed)
0.05" pins (low-speed)

This information is subject to change without notice

UDIMM Signal Access by SMP Connectors

| UDIMM Pin # | UDIMM Signal |
|-------------|--------------|
| 1 | VIN_BULK |
| 4 | HSCL |
| 5 | HSDA |
| 9 | DQ0_A |
| 11 | DQ1_A |
| 13 | DQS0_A_c |
| 14 | DQS0_A_t |
| 16 | DQ4_A |
| 18 | DQ5_A |
| 20 | DQ8_A |
| 22 | DQ9_A |
| 24 | DM1_A_n |
| 26 | DQ12_A |
| 28 | DQ13_A |
| 30 | DQ16_A |
| 32 | DQ17_A |
| 34 | DQS2_A_c |
| 35 | DQS2_A_t |
| 37 | DQ20_A |
| 39 | DQ21_A |
| 41 | DQ24_A |
| 43 | DQ25_A |
| 45 | DM3_A_n |
| 47 | DQ28_A |
| 49 | DQ29_A |
| 51 | CB0_A |
| 53 | CB1_A |
| 55 | DQS4_A_t |
| 56 | DQS4_A_c |
| 58 | CS0_A_n |
| 60 | CA0_A |
| 61 | CA2_A |
| 63 | CA4_A |
| 64 | CA6_A |
| 66 | CA8_A |
| 67 | CA10_A |
| 69 | CA12_A |

| UDIMM Pin # | UDIMM Signal |
|-------------|-----------------|
| 145 | VIN_BULK |
| 146 | VIN_BULK |
| 147 | PWR_GOOD/FAIL_n |
| 148 | HSA |
| 151 | PWR_EN |
| 154 | DQ2_A |
| 156 | DQ3_A |
| 158 | DM0_A_n |
| 160 | DQ6_A |
| 162 | DQ7_A |
| 164 | DQ10_A |
| 166 | DQ11_A |
| 168 | DQS1_A_c |
| 169 | DQS1_A_t |
| 171 | DQ14_A |
| 173 | DQ15_A |
| 175 | DQ18_A |
| 177 | DQ19_A |
| 179 | DM2_A_n |
| 181 | DQ22_A |
| 183 | DQ23_A |
| 185 | DQ26_A |
| 187 | DQ27_A |
| 189 | DQS3_A_c |
| 190 | DQS3_A_t |
| 192 | DQ30_A |
| 194 | DQ31_A |
| 196 | CB2_A |
| 198 | CB3_A |
| 200 | ALERT_n |
| 202 | CS1_A_n |
| 204 | CA1_A |
| 205 | CA3_A |
| 207 | CA5_A |
| 208 | CA7_A |
| 210 | CA9_A |
| 211 | CA11_A |

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UDIMM Signal Access (continued)

| UDIMM Pin # | UDIMM Signal |
|-------------|--------------|
| 72 | CK0_A_t |
| 73 | CK0_A_c |
| 78 | CK0_B_t |
| 79 | CK0_B_c |
| 82 | CA12_B |
| 84 | CA10_B |
| 85 | CA8_B |
| 87 | CA6_B |
| 88 | CA4_B |
| 90 | CA2_B |
| 91 | CA0_B |
| 93 | CS0_B_n |
| 95 | RESET_n |
| 97 | CB0_B |
| 99 | CB1_B |
| 101 | DQ0_B |
| 103 | DQ1_B |
| 105 | DQS0_B_c |
| 106 | DQS0_B_t |
| 108 | DQ4_B |
| 110 | DQ5_B |
| 112 | DQ8_B |
| 114 | DQ9_B |
| 116 | DM1_B_n |
| 118 | DQ12_B |
| 120 | DQ13_B |
| 122 | DQ16_B |
| 124 | DQ17_B |
| 126 | DQS2_B_c |
| 127 | DQS2_B_t |
| 129 | DQ20_B |
| 131 | DQ21_B |
| 133 | DQ24_B |
| 135 | DQ25_B |
| 137 | DM3_B_n |
| 139 | DQ28_B |
| 141 | DQ29_B |

| UDIMM Pin # | UDIMM Signal |
|-------------|--------------|
| 216 | CK1_A_t |
| 217 | CK1_A_c |
| 222 | CK1_B_t |
| 223 | CK1_B_c |
| 228 | CA11_B |
| 229 | CA9_B |
| 231 | CA7_B |
| 232 | CA5_B |
| 234 | CA3_B |
| 235 | CA1_B |
| 237 | CS1_B_n |
| 239 | DQS4_B_c |
| 240 | DQS4_B_t |
| 242 | CB2_B |
| 244 | CB3_B |
| 246 | DQ2_B |
| 248 | DQ3_B |
| 250 | DM0_B_n |
| 252 | DQ6_B |
| 254 | DQ7_B |
| 256 | DQ10_B |
| 258 | DQ11_B |
| 260 | DQS1_B_c |
| 261 | DQS1_B_t |
| 263 | DQ14_B |
| 265 | DQ15_B |
| 267 | DQ18_B |
| 269 | DQ19_B |
| 271 | DM2_B_n |
| 273 | DQ22_B |
| 275 | DQ23_B |
| 277 | DQ26_B |
| 279 | DQ27_B |
| 281 | DQS3_B_c |
| 282 | DQS3_B_t |
| 284 | DQ30_B |
| 286 | DQ31_B |

* Note: Pins not listed above are ground

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