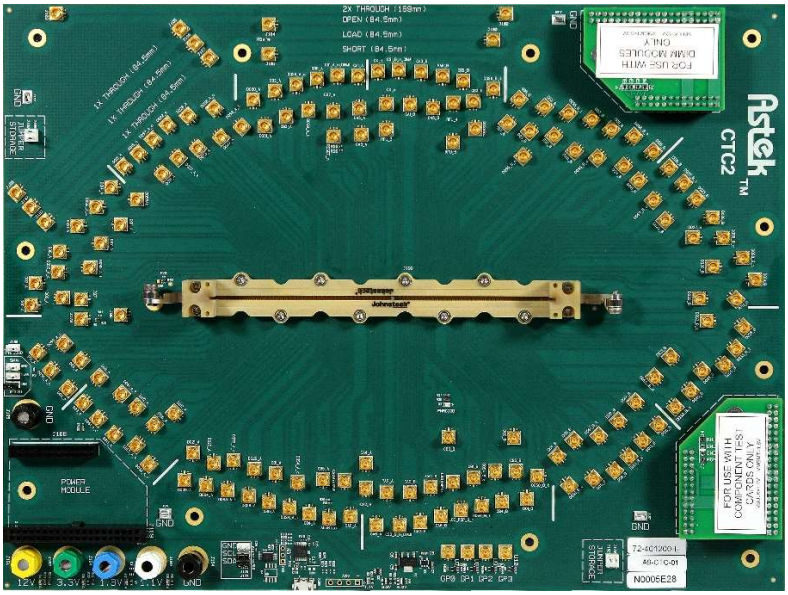
A9-xxx Controller Software

User Manual

Version: **June 16, 2022**



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1 Introduction / Overview

This document outlines the commands and scripts that are available for Astek's Controller software package. The first section outlines the CLI commands available for controlling the software and sending commands to the downstream device. The second section outlines a handful of .bat scripts that can be used to send a sequence of CLI commands to the to the downstream device.

2 Command Line Interface (CLI) Commands

Note: All values for address, data, rank, etc. are in hex format and a preceding 0x is not required.

Version

FORMAT:

Version <>

DESCRIPTION:

Display version of controller software.

ARGUMENTS:

Takes no arguments.

EXAMPLE:

DDR5Cntrl Version

Help

FORMAT:

Help [cmd]

DESCRIPTION:

When called with no arguments, displays all available commands. When called with an argument, displays format of the specified command.

ARGUMENTS:

cmd: Optional argument to get help about a specific command.

EXAMPLE:

DDR5Cntrl Help

DDR5Cntrl Help ReadByte

DramACT

FORMAT:

DramACT <devaddr> <devchan> <rank> <R> <BA> <BG> <CID> [R#]

DESCRIPTION:

Sends the Activate (ACT) command to a DRAM.

ARGUMENTS:

devaddr: Device address.

devchan: Desired device channel.

rank: Desired DRAM rank of 0 or 1.

R: Row Address

BA: Bank address

BG: Group bank address

CID: Chip ID

R#: When used, causes repeat to be set at # clocks.

Options are R2, R4, R8, 16, R64, R256, and R1024

EXAMPLE:

DDR5Cntrl DramACT 5A 0 1 05F8 2 3 1

DramWRP

FORMAT:

DramWRP <devaddr> <devchan> <rank> <BA> <BG> <CID> <C> [R#]

DESCRIPTION:

Sends the Write Pattern (WRP) command to a DRAM.

ARGUMENTS:

devaddr: Device address.

devchan: Desired device channel.

rank: Desired DRAM rank of 0 or 1.

BA: Banks address

BG: Group bank address

CID: Chip ID

C: Column Address

R#: When used, causes repeat to be set at # clocks.

Options are R2, R4, R8, R16, R64, R256, and R1024

EXAMPLE:

DDR5Cntrl DramWRP 5A 0 1 2 3 1 02F1

DramMRW

FORMAT:

DramMRW <devaddr> <devchan> <rank> <addr> <data> [R#]

DESCRIPTION:

Performs Mode Register Write (MRW) to a DRAM using VHOST mode. MRW occurs on the channel corresponding to chosen device channel (DevChan).

ARGUMENTS:

devaddr: Device address.

devchan: Desired device channel.

rank: Desired DRAM rank of 0 or 1.

addr: Address of mode register.

data: Data to write to mode register.

R#: When used, causes repeat to be set at # clocks.

Options are R2, R4, R8, R16, R64, R256, and R1024

EXAMPLE:

DDR5Cntrl DramMRW 5A 0 1 2B 58 R8

DDR5Cntrl DramMRW 64 1 1 4C 22

DramMRR

FORMAT:

DramMRR <devaddr> <devchan> <rank> <addr> [R#]

DESCRIPTION:

Performs Mode Register Read (MRR) to a DRAM using VHOST mode. MRR occurs on the channel corresponding to chosen device channel (DevChan).

ARGUMENTS:

devaddr: Device address.

devchan: Desired device channel.

rank: Desired rank of 0 or 1.

addr: Address of mode register.

R#: When used, causes repeat to be set at # clocks.

Options are R2, R4, R8, R16, R64, R256, and R1024

EXAMPLE:

DDR5Cntrl DramMRR 4B 0 1 2B R16

DDR5Cntrl DramMRR 55 1 1 4C

DramWR

FORMAT:

DramWR <devaddr> <devchan> <rank> <BA> <BG> <CID> <C> [R#]

DESCRIPTION:

Sends the Write (WR) command to a DRAM.

ARGUMENTS:

devaddr: Device address.

devchan: Desired device channel.

rank: Desired DRAM rank of 0 or 1.

BA: Banks address

BG: Group bank address

CID: Chip ID

C: Column Address

R#: When used, causes repeat to be set at # clocks.

Options are R2, R4, R8, R16, R64, R256, and R1024

EXAMPLE:

DDR5Cntrl DramWR 5A 0 1 2 3 1 0135

DramWRA

FORMAT:

DramWRA <devaddr> <devchan> <rank> <BA> <BG> <CID> <C> [R#]

DESCRIPTION:

Sends the Write with Auto Precharge (WRA) command to a DRAM.

ARGUMENTS:

devaddr: Device address.

devchan: Desired device channel.

rank: Desired DRAM rank of 0 or 1.

BA: Banks address

BG: Group bank address

CID: Chip ID

C: Column Address

R#: When used, causes repeat to be set at # clocks.

Options are R2, R4, R8, R16, R64, R256, and R1024

EXAMPLE:

DDR5Cntrl DramWRA 5A 0 1 2 3 1 002F

DramRD

FORMAT:

DramRD <devaddr> <devchan> <rank> <BA> <BG> <CID> <C> [R#]

DESCRIPTION:

Sends the Read (RD) command to a DRAM.

ARGUMENTS:

devaddr: Device address.

devchan: Desired device channel.

rank: Desired DRAM rank of 0 or 1.

BA: Banks address

BG: Group bank address

CID: Chip ID

C: Column Address

R#: When used, causes repeat to be set at # clocks.

Options are R2, R4, R8, R16, R64, R256, and R1024

EXAMPLE:

DDR5Cntrl DramRD 5A 0 1 2 3 1 0135

DramRDA

FORMAT:

DramRDA <devaddr> <devchan> <rank> <BA> <BG> <CID> <C> [R#]

DESCRIPTION:

Sends the Read with Auto Precharge (RDA) command to a DRAM.

ARGUMENTS:

devaddr: Device address.

devchan: Desired device channel.

rank: Desired DRAM rank of 0 or 1.

BA: Banks address

BG: Group bank address

CID: Chip ID

C: Column Address

R#: When used, causes repeat to be set at # clocks.

Options are R2, R4, R8, R16, R64, R256, and R1024

EXAMPLE:

DDR5Cntrl DramRDA 5A 0 1 2 3 1 0135

DramVrefCA

FORMAT:

DramVrefCA <devaddr> <devchan> <rank> <data> [R#]

DESCRIPTION:

Modifies the VrefCA setting on a DRAM using VHOST mode. VrefCA occurs on the channel corresponding to chosen device channel (DevChan).

ARGUMENTS:

devaddr: Address of target device.

devchan: Desired device channel.

rank: Desired DRAM rank of 0 or 1.

data: Data for VrefCA command.

R#: When used, causes repeat to be set at # clocks.

Options are R2, R4, R8, R16, R64, R256, and R1024

EXAMPLE:

DDR5Cntrl DramVrefCA 5A 0 1 24 R4

DDR5Cntrl DramVrefCA 5A 0 1 16

DramVrefCS

FORMAT:

DramVrefCS <devaddr> <devchan> <rank> <data> [R#]

DESCRIPTION:

Modifies the VrefCS setting on a DRAM using VHOST mode. VrefCS occurs on the channel corresponding to chosen device channel (DevChan).

ARGUMENTS:

devaddr: Address of target device.

devchan: Desired device channel.

rank: Desired DRAM rank of 0 or 1.

data: Data for VrefCS command.

R#: When used, causes repeat to be set at # clocks.

Options are R2, R4, R8, R16, R64, R256, and R1024

EXAMPLE:

DDR5Cntrl DramVrefCS 5A 0 1 39 R4

DDR5Cntrl DramVrefCS 5A 0 1 43

DramREFab

FORMAT:

DramREFab <devaddr> <devchan> <rank> <CID> [R#]

DESCRIPTION:

Sends the Refresh All (REFab) command to a DRAM.

ARGUMENTS:

devaddr: Device address.

devchan: Desired device channel.

rank: Desired DRAM rank of 0 or 1.

CID: Chip ID

R#: When used, causes repeat to be set at # clocks.

Options are R2, R4, R8, R16, R64, R256, and R1024

EXAMPLE:

DDR5Cntrl DramREFab 5A 0 1 1

DramRFMab

FORMAT:

DramRFMab <devaddr> <devchan> <rank> <CID> [R#]

DESCRIPTION:

Sends the Refresh Management All (RFMab) command to a DRAM.

ARGUMENTS:

devaddr: Device address.

devchan: Desired device channel.

rank: Desired DRAM rank of 0 or 1.

CID: Chip ID

R#: When used, causes repeat to be set at # clocks.

Options are R2, R4, R8, R16, R64, R256, and R1024

EXAMPLE:

DDR5Cntrl DramRFMab 5A 0 1 1

DramREFsb

FORMAT:

DramREFsb <devaddr> <devchan> <rank> <BA> <CID> [R#]

DESCRIPTION:

Sends the Refresh Same Bank (REFsb) command to a DRAM.

ARGUMENTS:

devaddr: Device address.

devchan: Desired device channel.

rank: Desired DRAM rank of 0 or 1.

BA: Banks address

CID: Chip ID

R#: When used, causes repeat to be set at # clocks.

Options are R2, R4, R8, R16, R64, R256, and R1024

EXAMPLE:

DDR5Cntrl DramREFsb 5A 0 1 2 1

DramRFMsb

FORMAT:

DramRFMsb <devaddr> <devchan> <rank> <BA> <CID> [R#]

DESCRIPTION:

Sends the Refresh Management Same Bank (RFMsb) command to a DRAM.

ARGUMENTS:

devaddr: Device address.

devchan: Desired device channel.

rank: Desired DRAM rank of 0 or 1.

BA: Banks address

CID: Chip ID

R#: When used, causes repeat to be set at # clocks.

Options are R2, R4, R8, R16, R64, R256, and R1024

EXAMPLE:

DDR5Cntrl DramRFMsb 5A 0 1 2 1

DramPREab

FORMAT:

DramPREab <devaddr> <devchan> <rank> <CID> [R#]

DESCRIPTION:

Sends the Precharge All (PREab) command to a DRAM.

ARGUMENTS:

devaddr: Device address.

devchan: Desired device channel.

rank: Desired DRAM rank of 0 or 1.

CID: Chip ID

R#: When used, causes repeat to be set at # clocks.

Options are R2, R4, R8, R16, R64, R256, and R1024

EXAMPLE:

DDR5Cntrl DramPREab 5A 0 1 1

DramPREsb

FORMAT:

DramPREsb <devaddr> <devchan> <rank> <BA> <CID> [R#]

DESCRIPTION:

Sends the Precharge Same Bank (PREsb) command to a DRAM.

ARGUMENTS:

devaddr: Device address.

devchan: Desired device channel.

rank: Desired DRAM rank of 0 or 1.

BA: Banks address

CID: Chip ID

R#: When used, causes repeat to be set at # clocks.

Options are R2, R4, R8, R16, R64, R256, and R1024

EXAMPLE:

DDR5Cntrl DramPREsb 5A 0 1 2 1

DramPREpb

FORMAT:

DramPREpb <devaddr> <devchan> <rank> <BA> <BG> <CID> [R#]

DESCRIPTION:

Sends the Precharge (PREpb) command to a DRAM.

ARGUMENTS:

devaddr: Device address.

devchan: Desired device channel.

rank: Desired DRAM rank of 0 or 1.

BA: Banks address

BG: Group bank address

CID: Chip ID

C: Column Address

R#: When used, causes repeat to be set at # clocks.

Options are R2, R4, R8, R16, R64, R256, and R1024

EXAMPLE:

DDR5Cntrl DramPREpb 5A 0 1 2 3 1

DramSRE

FORMAT:

DramSRE <devaddr> <devchan> <rank> [R#]

DESCRIPTION:

Sends the Self Refresh Entry (SRE) command to a DRAM.

ARGUMENTS:

devaddr: Device address.

devchan: Desired device channel.

rank: Desired DRAM rank of 0 or 1.

R#: When used, causes repeat to be set at # clocks.

Options are R2, R4, R8, R16, R64, R256, and R1024

EXAMPLE:

DDR5Cntrl DramSRE 5A 0 1

DramSREF

FORMAT:

DramSREF <devaddr> <devchan> <rank> [R#]

DESCRIPTION:

Sends the Self Refresh Entry with Frequency Charge (SREF) command to a DRAM.

ARGUMENTS:

devaddr: Device address.

devchan: Desired device channel.

rank: Desired DRAM rank of 0 or 1.

R#: When used, causes repeat to be set at # clocks.

Options are R2, R4, R8, R16, R64, R256, and R1024

EXAMPLE:

DDR5Cntrl DramSREF 5A 0 1

DramPDE

FORMAT:

DramPDE <devaddr> <devchan> <rank> [R#]

DESCRIPTION:

Sends the Power Down Entry (PDE) command to a DRAM.

ARGUMENTS:

devaddr: Device address.

devchan: Desired device channel.

rank: Desired DRAM rank of 0 or 1.

R#: When used, causes repeat to be set at # clocks.

Options are R2, R4, R8, R16, R64, R256, and R1024

EXAMPLE:

DDR5Cntrl DramPDE 5A 0 1

DramMPC

FORMAT:

DramMPC <devaddr> <devchan> <rank> <data> [R#]

DESCRIPTION:

Performs Multi-Purpose Command (MPC) to a DRAM using VHOST mode. MPC occurs on the channel corresponding to chosen device channel (DevChan).

ARGUMENTS:

devaddr: Device address.

devchan: Desired device channel.

rank: Desired DRAM rank of 0 or 1.

data: Data for MPC command.

R#: When used, causes repeat to be set at # clocks.

Options are R2, R4, R8, R16, R64, R256, and R1024

EXAMPLE:

DDR5Cntrl DramMPC 7C 0 1 58 R2

DDR5Cntrl DramMPC 2B 1 1 22

DramNOP

FORMAT:

DramNOP <devaddr> <devchan> <rank> [R#]

DESCRIPTION:

Performs No Operation (NOP) to a DRAM using VHOST mode. NOP occurs on the channel corresponding to chosen device channel (DevChan).

ARGUMENTS:

devaddr: Device address.

devchan: Desired device channel.

rank: Desired DRAM rank of 0 or 1.

R#: When used, causes repeat to be set at # clocks.

Options are R2, R4, R8, R16, R64, R256, and R1024

EXAMPLE:

DDR5Cntrl DramNOP 42 1 0 R1024

DDR5Cntrl DramNOP 3E 0 1

DramPDX

FORMAT:

DramPDX <devaddr> <devchan> <rank> [R#]

DESCRIPTION:

Sends the Power Down Exit (PDX) command to a DRAM.

ARGUMENTS:

devaddr: Device address.

devchan: Desired device channel.

rank: Desired DRAM rank of 0 or 1.

R#: When used, causes repeat to be set at # clocks.

Options are R2, R4, R8, R16, R64, R256, and R1024

EXAMPLE:

DDR5Cntrl DramPDX 5A 0 1

DramDES

FORMAT:

DramDES <devaddr> <devchan> [R#]

DESCRIPTION:

Sends Deselect (DES) command to a DRAM using VHOST mode. DES occurs on the channel corresponding to chosen device channel (DevChan).

ARGUMENTS:

devaddr: Device address.

devchan: Desired device channel.

R#: When used, causes repeat to be set at # clocks.

Options are R2, R4, R8, R16, R64, R256, and R1024

EXAMPLE:

DDR5Cntrl DramDES 42 1 R4

ReadDword

FORMAT:

ReadDword <devaddr> <devchan> <addr>

DESCRIPTION:

Reads the 4-byte aligned Dword containing the given address from the RCD.

ARGUMENTS:

devaddr: Address of target device.

devchan: Desired device channel.

addr: Address of the register to be written.
If a 2-byte address is used, the first byte is the page, and the second is the register to be written.
Address range is 0 - FFFF

EXAMPLE:

DDR5Cntrl ReadDword 5B 34 2A

DDR5Cntrl ReadDword 7D 6B 44

ReadByte

FORMAT:

ReadByte <devaddr> <devchan> <addr>

DESCRIPTION:

Reads the register at a given address from the RCD.

ARGUMENTS:

devaddr: Address of target device.

devchan: Desired device channel.

addr: Address of the register to be written.
If a 2-byte address is used, the first byte is the page, and the second is the register to be written.
Address range is 0 - FFFF

EXAMPLE:

DDR5Cntrl ReadByte 56 12 7

DDR5Cntrl ReadByte 2A 42 9B

WriteDword

FORMAT:

WriteDword <devaddr> <devchan> <addr> <byte1> ... <byte4>

DESCRIPTION:

Writes to the 4-byte aligned Dword containing the address to the RCD.

ARGUMENTS:

devaddr: Address of target device.

devchan: Desired device channel.

addr: Address of the register to be written.
If a 2-byte address is used, the first byte is the page, and the second is the register to be written.
Address range is 0 - FFFF

byte<n>: Hex value to be written to byte<n> of the selected page.

EXAMPLE:

DDR5Cntrl WriteDword 5F 1 B7 8A 51 FF A3

DDR5Cntrl WriteDword 2B 0 02 99 12 BA 3F

WriteWord

FORMAT:

WriteWord <devaddr> <devchan> <addr> <byte1> <byte2>

DESCRIPTION:

Writes to the Word starting at the given address to the RCD.

ARGUMENTS:

devaddr: Address of target device.

devchan: Desired device channel.

addr: Address of the register to be written.
If a 2-byte address is used, the first byte is the page, and the second is the register to be written.
Address range is 0 - FFFF

byte<n>: Hex value to be written to byte<n> of the selected page.

EXAMPLE:

DDR5Cntrl WriteWord 26 1 B7 8A 51

DDR5Cntrl WriteWord 7A 0 2 1099 12

WriteByte

FORMAT:

WriteByte <devaddr> <devchan> <addr> <byte>

DESCRIPTION:

Writes to the register at the given address to the RCD.

ARGUMENTS:

devaddr: Address of target device.

devchan: Desired device channel.

addr: Address of the register to be written.
If a 2-byte address is used, the first byte is the page, and the second is the register to be written.
Address range is 0 - FFFF

byte: Hex value to be written.

EXAMPLE:

DDR5Cntrl WriteByte 24 1 7 22

DDR5Cntrl WriteByte 3C 0 219B D1

I2CWriteByte

FORMAT:

I2cWriteByte <devaddr> <addr> <byte>

DESCRIPTION:

Writes to the I2C register at a given address.

ARGUMENTS:

devaddr: 7-bit device address of the memory to be written.

addr: Address of the I2C register to be written.

byte: Hex value to be written.

EXAMPLE:

DDR5Cntrl I2cWriteByte 5B 7 22

DDR5Cntrl I2cWriteByte 48 32 80

I2CReadByte

FORMAT:

I2cReadByte <devaddr> <addr>

DESCRIPTION:

Reads from the I2C register at a given address.

ARGUMENTS:

devaddr: 7-bit device address of the memory to be written.

addr: Address of the I2C register to be written.

EXAMPLE:

DDR5Cntrl I2cReadByte 5B 7

DDR5Cntrl I2cReadByte 22 32

SetGPIO

FORMAT:

SetGpio [#]... <on|off>

DESCRIPTION:

When called with only on|off, sets all pins to the desired value. When called with GPIO numbers, sets the selected pins to the desired value.

ARGUMENTS:

#: Optional argument that determines which pins (0-16) are affected.

on|off: Determined whether pins are turned on, or off.

EXAMPLE:

DDR5Cntrl SetGpio 0 2 3 off

DDR5Cntrl SetGpio on

Batch Scripts

The following are Windows batch scripts that can be used to issue a sequence of commands using the DDR5 Controller software

turnonpmic

DESCRIPTION: Writes the I2C register to turn on the PMIC.

initrcd

DESCRIPTION: Initializes the RCD to come out of reset. If the Reset Automation module is present, the script will bring the RCD out of reset prior to configuring.

noprcd

DESCRIPTION: Issues a sequence of three NOP commands to the RCD. This is only available with the Reset Automation module is present.

initdram

DESCRIPTION: Initializes the DRAM to come out of reset. Sets the termination impedance to 48-ohms for DQS and DQ signals. Turns off termination for the loopback pins.

pdaprogram

DESCRIPTION: Performs MRW commands to setup PDA programming for a single DRAM. The script will prompt the user when to apply the signals to the CTC2.

48ohm

DESCRIPTION: sets the termination impedance to 48-ohms for DQS and DQ signals.

lbrcd

DESCRIPTION: sets up loopback RCD.

lbdram

DESCRIPTION: sets up loopback for DQ0, channel A on the memory and configures the RCD to loopback the external signal to it’s loopback pin.

3 How to Contact Astek Corporation

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